WHAT IS CLAIMED:

1. A method of fabricating a semiconductor integrated circuit device comprising:

(a) forming a first insulting film and second insulating film over a first major surface of a wafer;

(b) forming a groove in the second insulating film and a hole in the first insulating film, the hole being connected to a bottom surface of the groove;

(c) performing an ammonia plasma treatment to an exposed surface in the groove and hole and a top surface of the second insulating film,

(d) forming a barrier metal film over inner surfaces of the groove and the hole and over an upper surface of the second insulating film;

(e) forming a copper seed layer over the barrier metal layer inside and outside the groove and the hole by copper sputtering with a copper target having a purity of 99.999% or more;

(f) forming a copper film containing copper as its principal component on the copper seed layer inside and outside the groove and the hole by electro plating so as to fill the groove and the hole;

(g) removing the barrier metal film, the copper seed layer and the copper film formed on the copper seed layer outside the groove and the hole so as to leave a copper interconnection in the groove and the hole, thereby exposing the first insulating film;

(h) performing an ammonia plasma treatment to the exposed surface of the first insulating film and an upper surface of the copper interconnection; and

(i) forming an insulating barrier film on the exposed surface of the first insulating film and the upper surface of the copper interconnection by plasma CVD.

2. The method of fabricating a semiconductor integrated circuit device as defined in Claim 1, wherein the purity of said copper target is not less than 99.9999%.

3. The method of fabricating a semiconductor integrated circuit device as defined in Claim 1, wherein the total concentration of components other than copper in the copper interconnection, when step (h) is completed, does not exceed 0.8At%.

4. The method of fabricating a semiconductor integrated circuit device as defined in Claim 3, wherein the total concentration of components other than copper does not exceed 0.08At%.

5. The method of fabricating a semiconductor integrated circuit device as defined in Claim 3, wherein the total concentration of components other than copper does not exceed 0.05At%.

6. The method of fabricating a semiconductor integrated circuit device as defined in Claim 3, wherein the total concentration of components other than copper does not exceed 0.02At%.

7. The method of fabricating a semiconductor integrated circuit device as defined in Claim 1, wherein the film thickness of the thinnest part of the barrier metal film in the groove and the hole is less than 10 nm.

8. The method of fabricating a semiconductor integrated circuit device as defined in Claim 7, wherein the film thickness is not more than 3nm.

9. The method of fabricating a semiconductor integrated circuit device as defined in Claim 7, wherein the film thickness is not more than 2nm, or there is no metal barrier film.

10. The method of fabricating a semiconductor integrated circuit device as defined in Claim 1, wherein a width of said groove does not exceed 0.4μm.

11. The method of fabricating a semiconductor integrated circuit device as defined in Claim 1, wherein a width of said groove does not exceed 0.25μm.

12. The method of fabricating a semiconductor integrated circuit device as defined in Claim 1, wherein a width of said groove does not exceed 0.2μm.

13. A method of fabricating a semiconductor integrated circuit device comprising:

(a) forming a first insulating film and second insulating film over a first major surface of a wafer;

(b) forming a groove in the second insulating film and a hole in the

first insulating film, the hole being connected to a bottom surface of the groove;

(c) performing an hydrogen plasma treatment to an exposed surface in the groove and hole and a top surface of the second insulating film;

(d) forming a barrier metal film over inner surface of the groove and the hole and over an upper surface of the second insulating film;

(e) forming a copper seed layer over the barrier metal layer inside and outside the groove and the hole by copper sputtering with a copper target having a purity of 99.999% or more;

(f) forming a copper film containing copper as its principal component on the copper seed layer inside and outside the groove and the hole by electro plating so as to fill the groove and the hole;

(g) removing the barrier metal film, the copper seed layer and the copper film formed on the copper seed layer outside the groove and the hole so as to leave a copper interconnecting in the groove and the hole, thereby exposing the first insulating film;

(h) performing an ammonia plasma treatment to the exposed surface of the first insulating film and an upper surface of the copper interconnection; and

(i) forming an insulating barrier film on the exposed surface of the first insulating film and the upper surface of the copper interconnection by plasma CVD, wherein the total concentration of components other than copper in the copper interconnection, when step (h) is completed, does not exceed 0.8At%.

14. The method of fabricating a semiconductor integrated circuit device as defined in Claim 13, wherein the purity of said copper target is not less than 99.9999%.

15. The method of fabricating a semiconductor integrated circuit device as defined in Claim 13, wherein the total concentration of components other than copper does not exceed 0.2At%.

16. The method of fabricating a semiconductor integrated circuit device as defined in Claim 13, wherein the total concentration of components other than copper does not exceed 0.08At%.

17. The method of fabricating a semiconductor integrated circuit device as defined in Claim 13, wherein the total concentration of components other than copper does not exceed 0.05At%.

18. The method of fabricating a semiconductor integrated circuit device as defined in Claim 13, wherein the film thickness of the thinnest part of the barrier metal film in the groove and the hole is less than 10 nm.

19. The method of fabricating a semiconductor integrated circuit device as defined in Claim 18, wherein the film thickness is not more than 5 nm.

20. The method of fabricating a semiconductor integrated circuit device as defined in Claim 18, wherein the film thickness is not more than 2nm, or there

is no metal barrier film.